Collins, Colorado 80527-2400

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):

Padmanabha I. VENKITAKRISHNAN, et al.

Confirmation No.: 8711

Application No.: 09/916,598

Examiner: Knoll, C. H.

Filing Date:

07/26/01

Group Art Unit: 2112

Title:

A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS ARCHITECTURE AND

PROTOCOL FOR A MULTI PROCESSOR CHIP DEVICE

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME

Sir:

In an Office Action mailed on01/05/05, on the above-identified U.S. Patent
application, a shortened statutory period of3 months was set for response. In accordance
with 37 C.F.R. 1.136(a), applicant(s) hereby request(s) a:
(X) one month
() two months
() three months
() four months
time extension so that the period for response to the Office Action expires on
Authorization to charge the fee required by 37 CFR 1.17 to Deposit Account $23-0085$ appears in the
enclosed transmittal letter. At any time during the pendency of this application, please charge any
fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.
Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21
inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate
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Date of Deposit: 05/05/05

Typed Name: Desiree Reardon

Respectfully submitted,

Padmanabha I. VENKITAKRISHNAN, et

John P. Wagner, Jr.

Attorney/Agent for Applicant(s)

Reg. No. 35,398

Date: 05/05/05

Telephone No.: (408) 938-9060